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1	BRS	L1	1011	703/14.ccls.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 14:47

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1	BRS	L1	2	"6573744".pn.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:12
2	BRS	L2	92	tsai-r.in.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:15
3	BRS	L3	5175	(bias same dependence)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:32
4	BRS	L4	242	(bias adj dependence)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:33
5	BRS	L5	11	(bias adj dependence) same temperature same process	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:35

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6	BRS	L6	90	(semiconductor) and (bias adj dependence) and (temperature) and process	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:36
7	BRS	L7	3	(semiconductor) and (bias adj dependence) and (temperature) and process and (lay adj out)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:47
8	BRS	L8	45194	(semiconductor) same subsequent	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:47
9	BRS	L9	5	((semiconductor) same subsequent) and (s-parameter)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:48
10	BRS	L10	1	((semiconductor) same subsequent) and (s-parameter) and SEM	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:48

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11	BRS	L11	3	((semiconductor) same subsequent) and (s-parameter) and (semiconductor same characteristics)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:48
12	BRS	L12	3	((semiconductor) same subsequent) and (s-parameter) and (semiconductor same characteristics) and fabrication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
13	BRS	L13	1	((semiconductor) same subsequent) and (equivalent adj model) and (semiconductor same characteristics) and fabrication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
14	BRS	L14	2	((semiconductor) same subsequent) and (equivalent adj model) and fabrication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
15	BRS	L15	85	((semiconductor) same subsequent) and (equivalent same model) and fabrication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:52

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	4	((semiconductor) same subsequent) and (equivalent same model same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
17	BRS	L17	163	(equivalent same model same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
18	BRS	L18	1	((equivalent adj model) same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
19	BRS	L19	100	((equivalent adj model) and fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:56
20	BRS	L20	16	((equivalent adj model) same semiconductor)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:56

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21	BRS	L21	0	((equivalent adj model) same semiconductor) and subsequejt	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:57
22	BRS	L22	5	((equivalent adj model) same semiconductor) and subsequent	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:29
23	BRS	L23	2	"5878053".pn.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:31
24	BRS	L24	1	"5878053".pn. and average	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:42
25	BRS	L25	1	"5878053".pn. and characteristics	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 11:03

	Type	L #	Hits	Search Text	DBs	Time Stamp
26	BRS	L26	1	"5878053".pn. and sample	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 11:03



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J Nasrullah, JB Burr, GL Tyler - Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE ..., 2003 - [ieeexplore.ieee.org](#)

... 400mT, 1400W RF power, and electrode **bias** of — 530V ... Their **process** used high-temperature oxide for the etch ... such as this edge-defined **process** potentially offer ...

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ESD Scalability of LDMOS Devices for Self-Protected Output Drivers

Y Chung, H Xu, R Ida, WG Min, B Baird - Power Semiconductor Devices and ICs, 2005. Proceedings. ..., 2005 - [ieeexplore.ieee.org](#)

... grounded-gate (gg) condition, junction **temperature** profile within ... 1000u, as a function of the gate **bias**. ... geometries under snapback breakdown **process** has been ...

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RHEA (resist-hardened etch and anodization) process for fine-geometry Josephson junction fabrication - group of 2 »

LPS Lee, ER Arambula, G Hanaya, C Dang, R Sandell, ... - Magnetics, IEEE Transactions on, 1991 - [ieeexplore.ieee.org](#)

... CD with a constant CD **bias** improves the ... and J. Pacansky, "High Temperature Flow Resistance ... Jiltie, "Selective niobium anodization **process** for fabricating ...

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Mechanical Stress Induced MOSFET Punch-through And Process Optimization For Deep Submicron TEOS-O/ ...

K Ishimaru, F Matsuoka, M Takahashi, M Nishigohri, ... - VLSI Technology, 1997. Digest of Technical Papers., 1997 ..., 1997 - [ieeexplore.ieee.org](#)

... Optimized high **temperature** annealing achieved defect free characteristics and ... **Process** integration for future STI devices should take ... 6 8 1 0 Reverse **Bias** (V) (b ...

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An ultra dense trench-gated power MOSFET technology using a self-aligned process

J Zeng, G Dolny, C Kocon, R Stokes, N Kraft, L ... - Power Semiconductor Devices and ICs, 2001. ISPSD'01. ..., 2001 - [ieeexplore.ieee.org](#)

... The **process** and physical models, as well as ... **temperature** gate **bias** (HTGB), humidity **bias**, autoclave, **temperature** ... level at the zero **temperature**-coefficient point ...

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Sensors and the Influence of Process Parameters and Thin Films - group of 2 »

HR Krauss - ADVANCES IN SOLID STATE PHYSICS-PERGAMON PRESS THEN VIEWEG-, 2002 - Springer ... 6). After **process** related **temperature** treatment voids are formed ... polysilicon layer,

V is the **bias** voltage across ... **scale** regions and to get **process** tolerances by ...

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MEMS Packaging on a Budget (Fiscal and Thermal)

MB Cohn, R Roehneilt, JH Xu, A Shteinberg, S Cheung ... - [ieeexplore.ieee.org](#)

... up to 5 RF interconnects, and 4 **bias** connections ... can be performed within the back-end **temperature** range of ... values are on par with those of a monolithic **process**. ...

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No-Fault Assurance: Linking Fast **Process** CAD and EDA - group of 2 »

A Neureuther, F Gennari - Proc. SPIE, 2002 - eecs.berkeley.edu

... **Bias** ... The accuracy of this **temperature** cooling estimate is obviously rather ... be used to communicate among circuit designers, mask makers and **process** technologists ...

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Vertical sige-base bipolar transistors on cmos-compatible soi substrate

J Cai, M Kumar, M Steigerwalt, H Ho, K Schonenberg ... - Bipolar/BiCMOS Circuits and Technology Meeting, 2003. ..., 2003 - ieeexplore.ieee.org

... by varying collector doping, **layout** and SQL substrate **bias**. ... that of a bulk SiGe bipolar **process** [6]. An ... stack, using the UHV/CVD Low-Temperature-Epitaxy (LTE ...

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Fabricating 90 nm Devices by 2004

S Equipment - kla-tencor.com

... replicate the customers' design rules and **bias**," said KLA's ... In the S/D, the **process** calls for ... preferably with instantaneous time-at-**temperature** (spike anneal ...

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... CA 90278 Tel: (310) 812-8254, Fax: (310) 813-0418, Email: **roger.tsai@trw.com** ... If we
trusted our **S- parameter** measurements up to only 50 GHz, customers doing V ...
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M Gleicher, A Witkin - ACM SIGGRAPH Computer Graphics, 1992 - portal.acm.org
... Because the error norm of equation 6 is the Euclidean distance in the camera's
parameter space, rather than being intrinsic to the world-space camera motion ...
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PA Pittsburgh - cs.princeton.edu
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